Abstracts

50-GHz interconnect design in standard silicon technology

B. Kleveland, T.H. Lee and S.S. Wong. "50-GHz interconnect design in standard silicon technology." 1998 MTT-S International Microwave Symposium Digest 98.3 (1998 Vol. III [MWSYM]): 1913-1916.

Coplanar waveguides were fabricated in a process that emulates silicon CMOS technologies with 5 to 10 metal layers. The observed S/sub 21/ loss of 0.3 dB/mm at 50 GHz is among the lowest ever reported with standard Al interconnects on Si/SiO/sub 2/. Optimum design parameters were counter-intuitive: in some frequency ranges, the lowest loss was achieved with relatively narrow lines over a low-resistivity substrate. This was exploited in the design of transmission lines that are fully compatible with a CMOS technology. The process emulation was calibrated with a commercial 4-layer Al/Cu CMOS technology.

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